What is claimed is:

1. A circuit for analog-to-digital conversion, comprising:

a fine channel circuit that includes folding stages;

a coarse channel circuit; and

a coarse channel calibration circuit that is coupled to the coarse channel circuit.

2. The circuit of Claim 1, further comprising:

a control circuit that is configured to provide a select signal; and

a voltage reference circuit that is configured to provide a voltage reference signal that corresponds to the select signal, wherein

the coarse channel circuit is configured to receive the voltage reference signal.

3. The circuit of Claim 1,

wherein the coarse channel circuit is configured to provide an output signal in response to a voltage reference signal, and

wherein the coarse channel calibration circuit is configured to:

receive a feedback signal from the coarse channel circuit, and

provide an adjustment signal to the coarse channel circuit in response to the feedback signal.

4. The circuit of Claim 1,

wherein the coarse channel circuit comprises an amplifier array and a comparator array, and

wherein at least one of the amplifier array and the comparator array is configured to receive the adjustment signal.

5. The circuit of Claim 3,

wherein the output signal includes the feedback signal.

6. The circuit of Claim 1,

wherein the coarse channel calibration circuit includes:

a counter circuit that is coupled to the coarse channel circuit; and

a parameter adjustment circuit that is coupled to the counter circuit and the coarse channel circuit.

7. The circuit of Claim 6,

wherein the parameter adjustment circuit includes a digital-to-analog converter circuit, and

wherein the digital-to-analog converter circuit is configured to provide a converted signal to the coarse channel circuit.

8. The circuit of Claim 6, wherein

the coarse channel circuit is configured to provide a feedback signal,

the counter circuit is configured to:

receive the feedback signal, and

provide a count signal in response to the feedback signal, and wherein the parameter adjustment circuit is configured to:

receive the count signal, and

adjust a parameter of the coarse channel circuit in response to the count signal.

9. The circuit of Claim 8,

wherein the parameter comprises one of a single-ended current and differential current.

10. The circuit of Claim 8,

wherein the counter circuit is configured to, if latched:

increment a count value that is associated with the count signal if the comparator output corresponds to a first logic level, and

decrement the count value if the comparator output corresponds to a second logic level.

11. The circuit of Claim 8,

wherein the parameter adjustment circuit includes:

a first digital-to-analog converter circuit that is configured to convert the count signal into a first analog signal; and

a second digital-to-analog converter circuit that is configured to convert an inverted count signal into a second analog signal.

12. The circuit of Claim 11, wherein

the coarse channel circuit includes an amplifier that is configured to provide a differential output current,

the amplifier includes:

a first load that is configured to receive a first half of the differential output current and the first analog signal; and

a second load that is configured to receive a second half of the differential output current and the second analog signal,

the first current digital-to-analog converter circuit is configured to provide the first analog signal to the first load, and wherein

the second current digital-to-analog converter circuit is configured to provide the second analog signal to the second load.

13. The circuit of Claim 12, wherein

the first current digital-to-analog converter circuit includes:

a first current digital-to-analog converter; and

a first transistor that is coupled between the first current digital-to-analog converter and the first load,

the second current digital-to-analog converter circuit includes:

a second current digital-to-analog converter; and

a second transistor that is coupled between the first current digital-to-analog converter and the first load, and wherein

the first and second transistors are each configured to operate as cascode transistors.

14. The circuit of Claim 1, further comprising:

a control circuit that is configured to:

provide a select signal; and

provide a timing signal at a pre-determined amount of time after providing the select signal,

wherein the coarse channel circuit is configured to provide an output signal, and

wherein the coarse channel calibration circuit is configured to latch the output signal in response to the timing signal.

15. A circuit for calibration in a folding analog-to-digital conversion architecture, the circuit comprising:

a coarse channel calibration circuit that is configured to:

receive an output signal from a coarse channel circuit of a folding analog-to-digital converter circuit; and

adjust a parameter of the coarse channel circuit in response to the output signal.

16. The circuit of Claim 15, further comprising:

a control circuit that is arranged to:

provide a select signal for selecting a voltage reference; and

assert a timing signal for latching the coarse channel calibration circuit at a pre-determined amount of time after a change of the select signal.

17. The circuit of Claim 15,

wherein the coarse channel calibration circuit includes:

a counter circuit that is configured to provide a count signal in response to the timing signal and the output signal; and

a parameter adjustment circuit that is configured to adjust the parameter in response to the count signal.

18. A method for coarse channel calibration in a folding analog-to-digital conversion architecture, the method comprising:

providing a reference voltage to a coarse channel circuit of a folding analog-to-digital converter circuit; and

adjusting a parameter of the coarse channel circuit until an output of the coarse channel circuit is calibrated in relation to the reference voltage.

19. The method of Claim 18, further comprising:

receiving a signal from the coarse channel circuit after providing the reference voltage; and

adjusting a count in response to the signal,

wherein the parameter is adjusted according to the count.

20. A circuit with an analog-to-digital conversion architecture, comprising:

means for providing a fine channel circuit with a folding analog-to-digital converter architecture;

means for providing a coarse channel circuit; and

means for calibrating the coarse channel circuit.